27.2 A 65nm Embedded SRAM with Wafer-Level Burn-In Mode, Leak-Bit Redundancy and E-Trim Fuse for Known Good Die

Shigeki Ohbayashi[1], Makoto Yabuuchi[1], Kazushi Kono[1], Yuji Oda[2], Susumu Imaoka[3], Keiichi Usui[4], Toshiaki Yonezu[1], Takeshi Iwamoto[1], Koji Nii[1], Yasumasa Tsukamoto[1], Masashi Arakawa[1], Takahiro Uchida[1], Masakazu Okada[1], Atsushi Ishii[1], Hiroshi Makino[1], Koichiro Ishibashi[1], Hirofumi Shinohara[1]

[1]Renesas Technology, Itami, Japan, [2]Shikino High-Tech, Osaka, Japan
[3]Renesas Device Design, Itami, Japan, [4]Daioh Electric, Itami, Japan

Recently, digital electronics have achieved higher performance from the progress of both CMOS and packaging technologies that integrate multiple chips into one package, such as MCM, SiP and system-on-package (SoP) [1]. The advance of known good die (KGD) technology is essential [2] to keeping the cost low of these packaging technologies. In this paper, we propose a wafer-level burn-in (WLBI) mode, leak-bit redundancy and a small e-trim fuse circuit for embedded 6T SRAM to achieve a low-cost KGD.

Figure 27.2.1 shows the proposed low cost KGD test flow chart at high temperature, and a block diagram of the key techniques of the low cost KGD test flow. The KGD test flow includes several temperature wafer probe tests. We call the operational 6T cell with abnormal leak current a *leak bit*. The leak current of the leak bits results from defects causing short circuits. The leak bits become early-failure 6T-cells in many cases, so the leak bits worsen the infant mortality of products. We need to find early-failure 6T cells using WLBI in a very short time using stronger stress than conventional burn-in (BI). Early-failure 6T cells become fail bits and also leak bits in the WLBI. Conventionally, leak bits cannot be replaced by spare rows or columns because their address cannot be identified. The proposed leak bit redundancy presents a way to determine the address of the leak-bits by turning them into fail addresses. Therefore, repairing, with e-trim fuses [3], BI failures and other failures including leak bits reduces the infant mortality of bare chips.

In the block diagram, the WLBI mode, the leak-bit redundancy and the e-trim fuse are implemented on the SRAM using a capacitive write-assist circuit [4]. "WA Cir." means a write assist circuit and "BL Load" means a bitine load. CRED_N is generated in the spare column control circuit. BI_W_N and BI_MODE are the signals related to the WLBI mode. RED_LEAK1, RED_LEAK2 and RED_LEAK3 are the signals related to the leak-bit redundancy.

Figure 27.2.2 shows the WLBI mode operation. V_{DD} above 2.0V is essential in the WLBI mode because a stress comparable with the conventional BI is applied in a very short period (around 10 sec) to 1.2V core transistors. The bitline load is inactive and the operation of the write-assist circuit is simple because BI_MODE is high during the WLBI mode. Even WLs and odd WLs are alternately active because the stress is applied between even WLs and odd WLs in the WLBI mode. If many WLs are simultaneously active and all BL pairs are set to either "0/1" or "1/0" in a 6T SRAM, the write operation is impossible due to the huge current between vast numbers of simultaneously active load PMOSs and the NMOSs of the write drivers. However, all arvdd lines are lowered to around $|V_{tp}|$ through load PMOSs and access NMOSs of active 6T cells when BI_W_N is low in the WLBI mode all BLs and #BLs are simultaneously lowered to GND. Then all arvdd lines are charged to around half-Vdd by "H" data given to either BLs or #BLs through the load PMOSs and the access NMOSs. Finally, all arvdd lines are charged to V_{DD} when BI_W_N is high. Using the WLBI mode enables the simultaneous write operation of vast numbers of 6T cells without a penetrating current.

Fig. 27.2.3 shows the leak-bit redundancy operation. In State A, P1 is OFF, leak judging switches are ON, the leak column latch circuit is active and all arvdd lines and BL pairs are floating because the bitline load and write assist are inactive. The leak-judging node is connected to all arvdd lines and BL pairs of this spare column unit. Node-Out is low and the leak judging circuit is inactive because RED_LEAK2 is low. When leak bits exist in this spare column unit, the floating leak judging node is lowered to less than the threshold voltage of the leak judging circuit. In State B, because the leak judging circuit and N1 of the leak column latch circuit are active, Node-Out changes to "H" due to the leak-judging node being lowered to GND by N2 when leak-bits exist. In State C, Node-Out is low when no leak-bits exist. In this case, V_{DD} is supplied to this spare column unit. On the other hand, the write assists and the bitline loads of this spare column unit are inactive because Node-Out is high when leak-bits exist. Therefore, if one or more leak bits exist in one spare column unit, it fails the function test in State C.

Figure 27.2.4 shows the Cu e-trim fuse circuit, layout and cross-section. We use only 1.2V core transistors in the Cu e-trim fuse circuit. Therefore, the size will shrink with CMOS technology scaling. We achieve the small e-trim fuse circuit size of $6\times36\mu m^2$, which is comparable with that of a laser-blown fuse. That is because the trimming current supply circuit is placed under our crack-less Cu e-trim fuse [3] with 65nm technology. The scheme was not reported in previous papers [3,5]. The following three techniques enable this stacked structure: (i) The walls formed by the gutter-shaped via and the Cu wiring are placed around the fuse. (ii) Virtual GND (V_GND) and Node-N are set to V_{DD} except when trimming and trimming judging. (iii) The p-well of the NMOS transistors under the e-trim fuse is separated with a p-substrate using a triple well. The infection of Cu thermal and bias diffusions is suppressed by (i) and (ii). The abnormal gate leak current of the transistors under the fuse by trimming damage and Cu diffusion does not affect the total current of the e-trim fuse circuit because of (iii).

Figure 27.2.5 shows the evaluation results of the WLBI mode. The fail bit map (FBM) enlarged one portion of 4M SRAM of $0.494\mu m^2$ cells becomes a row-stripe using the WLBI mode. Therefore, we confirm that the simultaneous write operation was enabled. The WLBI mode has almost no area penalty and only around 50ps of speed penalty because one NOR gate stage is added to the pre-decoders. From the difference of the wafer FBM (WFBM) of the 4M SRAM between before and after the BI stress, we confirm that row and column failures increase in the WLBI mode because the row stress increases 256× and the column stress increases 1024× compared with the conventional write. The BI stress condition of this experiment is much stronger than that of mass production.

Figure 27.2.6 shows the evaluation results of the leak bit redundancy. We used a wafer whose standby current distribution was worse than usual by a certain wafer-process experiment in this experiment. The standby current distribution of the 4M SRAM using $0.494\mu m^2$ cells improves using this technique. From the difference in the WFBM of this 4M SRAM before and after using this technique, we confirm that the technique increases repair column unit failures. The area penalty of this technique is less than 2%.

We fabricated a 16M SRAM [4] by implementing the WLBI mode, the leak-bit redundancy and the e-trim fuse with 65nm LSTP technology. Figure 27.2.7 shows a 16M SRAM micrograph and an SEM photograph of the e-trim fuse. Each 512K SRAM macro has 35 e-trim fuses. Each e-trim fuse has walls on both sides of the 8μm length fuse formed by the Cu wiring.

References:

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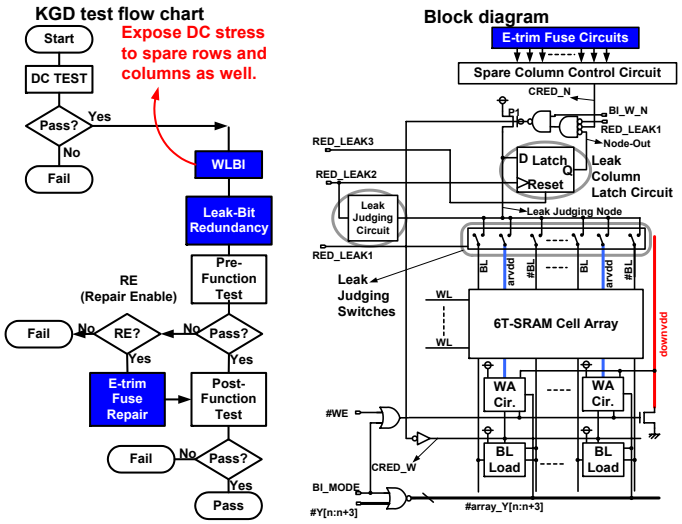


Figure 27.2.1: Proposed KGD test flow chart and block diagram of key techniques.

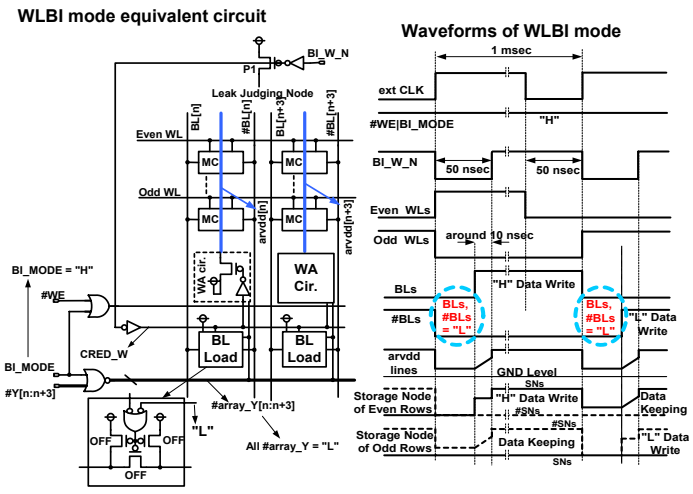


Figure 27.2.2: WLBI mode operation.

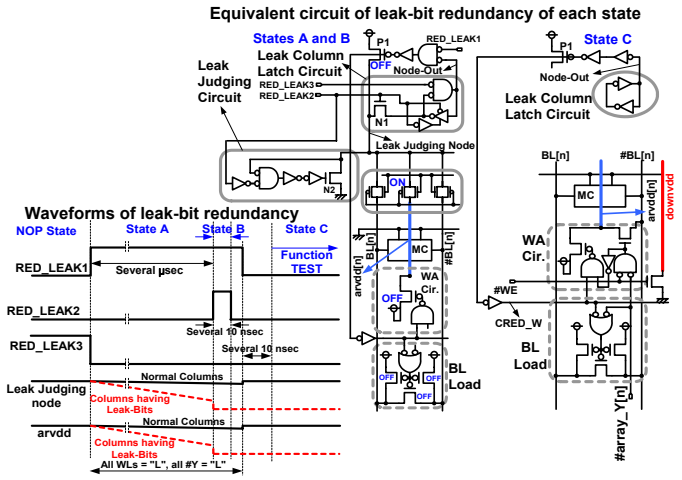


Figure 27.2.3: Leak-bit redundancy operation.

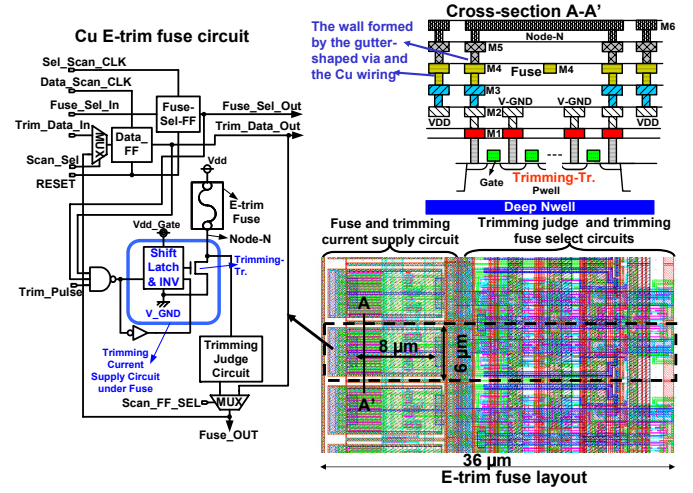


Figure 27.2.4: Cu e-trim fuse circuit, layout and cross-section.

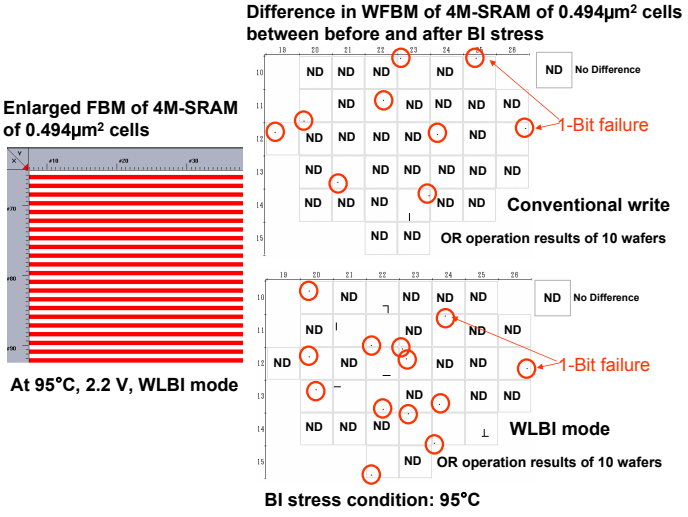


Figure 27.2.5: Evaluation results of WLBI mode.

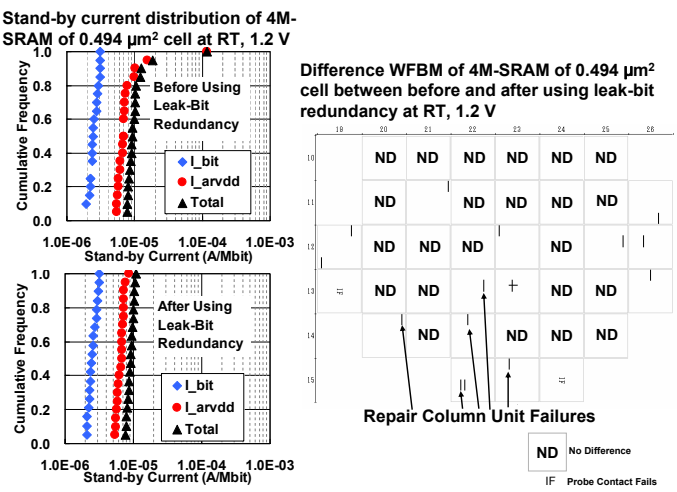
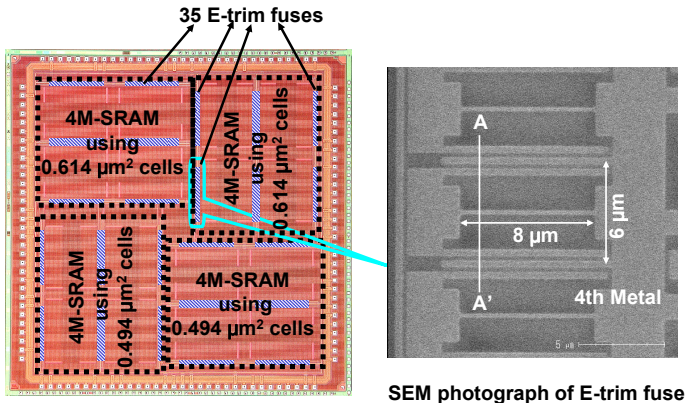


Figure 27.2.6: Evaluation results of leak-bit redundancy.

Continued on Page 617



Micrograph of 16M SRAM that includes 8M SRAM of 0.494µm² cells and 8M SRAM of 0.614µm² cells

SEM photograph of E-trim fuse

Figure 27.2.7: Chip micrograph and SEM photograph of e-trim fuse.

